IN THE CLAIMS

Please amend the claims as follows.

1. (currently amended) A method for manufacturing a silicon wafer, in which a silicon crystal is pulled from a silicon melt, and a silicon wafer is acquired from the pulled silicon crystal, the method comprising:

Pulling up the silicon crystal while keeping within a range of

~~wherein the silicon crystal is pulled up by lowering~~ a growth condition V/G_1 (V: growth rate, G_1: axial temperature gradient near a melting point of the silicon crystal) defining a range of ~~to~~ near a critical value in which there is an effect that a size of the void defect becomes smaller, and which is a range that is larger than a critical value of a void defect region and an OSF (Oxygen Induced Stacking Faults) region; and in a state in which the axial temperature gradient G_1 near the melting point of the silicon crystal is increased and a solid-liquid interface, which is a boundary between the silicon crystal and the melt during the pulling of the silicon crystal, is convex with respect to the melt surface.

2. (currently amended) The method for manufacturing a silicon wafer according to Claim 1, wherein a cooler is used to cool the silicon crystal, ~~thereby lowering the growth condition V/G_1 to near the critical value~~ while keeping a growth condition V/G_1 within the range of near a critical value in a state in which the solid-liquid interface is convex with respect to the melt surface within a range in which the growth rate V is from 75 to 97% of Vmax (the limit growth rate at which growth is possible without deformation of the silicon crystal), and the silicon crystal is pulled in which no OSF (oxidation induced stacking fault) region is present anywhere in the plane of the silicon wafer.

3. (currently amended) The method for manufacturing a silicon wafer according to Claim 1, wherein a cooler is used to cool the silicon crystal, ~~thereby lowering the growth condition V/G_1 to near the critical value~~ while keeping a growth condition V/G_1 within the range of near a critical value in the state in which the axial temperature gradient G_1 near the melting point of the silicon crystal is increased.

4. (original) The method for manufacturing a silicon wafer according to Claim 1, wherein a magnetic field is applied to the silicon melt to make the solid-liquid interface convex

with respect to the melt surface.

5. (original) The method for manufacturing a silicon wafer according to Claim 1, wherein a cooler is used to cool the silicon crystal, and a rotational speed of the silicon crystal, or a rotational speed of the crucible containing the silicon melt, is adjusted, thereby making the solid-liquid interface convex with respect to the melt surface.

6. (currently amended) A method for manufacturing a silicon wafer, in which a silicon crystal is pulled from a silicon melt, and a silicon wafer is acquired from the pulled silicon crystal, the method comprising:

Pulling the silicon crystal while keeping the growth condition V/G_1 within a range of a growth condition V/G_1 (V/: is a growth rate of the pulled silicon crystal, G_1: is an axial temperature gradient near a melting point of the silicon crystal), defining a range of near a critical value in which there is an effect that a size of a void defect becomes smaller and no OSF (Oxidation Induced Stacking Fault) region is present in a plane of the silicon wafer at least from a center of the lane up to 10 mm from an outer periphery and which is a range in a void defect region and the OSF region; and wherein the silicon crystal is pulled in a state in which the axial temperature gradient G_1 near a melting point of the silicon crystal has been increased by cooling the silicon crystal with the use of a cooler.

~~wherein a cooler is used to cool the silicon crystal, thereby lowering a growth condition V/G_1 to near a critical value in a state in which the axial temperature gradient G_1 near a melting point of the silicon crystal has been increased, and the silicon crystal is pulled in which no OSF (oxidation induced stacking fault) region is present in a plane of the silicon wafer at least from a center of the plane up to 10 mm from an outer periphery.~~

7. (currently amended) The method for manufacturing a silicon wafer according to Claim 6, wherein an oxygen concentration in the silicon crystal is controlled to be not more than 12.5×10^{17} atoms/cm^3 ~~(Year 1979 ASTM)~~.

8. (original) The method for manufacturing a silicon wafer according to Claim 6, wherein the silicon wafer is subjected to heat treatment at 1000°C or higher so that OSF nuclei will not materialize as OSFs in the silicon wafer.

9. (original) The method for manufacturing a silicon wafer according to Claim 6,

wherein the silicon wafer is subjected to heat treatment at 1000°C or higher in a non-oxidative atmosphere so that OSF nuclei will not materialize as OSFs in the silicon wafer and so that void defects will be eliminated in the silicon wafer surface layer.

10. (cancelled)

11. (cancelled)

12. (cancelled)

13. (currently amended) The ~~apparatus~~ method for manufacturing a silicon wafer according to Claim [10] 3, wherein the cooler is disposed so as to surround the silicon crystal at a distance of 30 to 500 mm from the silicon melt.

14. (currently amended) The ~~apparatus~~ method for manufacturing a silicon wafer according to Claim [12] 6, wherein the cooler is disposed so as to surround the silicon crystal at a distance of 30 to 500 mm from the silicon melt.

15. (currently amended) The ~~apparatus~~ method for manufacturing a silicon wafer according to Claim [10] 3, wherein a heat shield is provided above the silicon melt, and a gap between a lower end of the heat shield and the silicon melt surface is set to between 20 and 100 mm.

16. (currently amended) The ~~apparatus~~ method for manufacturing a silicon wafer according to Claim [12] 6, wherein a heat shield is provided above the silicon melt, and a gap between a lower end of the heat shield and the silicon melt surface is set to between 20 and 100 mm.

17. (cancelled)

18. (cancelled)

19. (currently amended) A method for manufacturing a defect-free silicon single crystal in which void defects, OSFs (oxidation induced stacking faults), and dislocation clusters

(interstitial silicon dislocation defects) have been eliminated by setting a carbon concentration to 1×10^{15} atoms/cm^3 or less and adjusting a growth condition V/G (V: growth rate, G: axial temperature gradient of the crystal).

20. (cancelled)

21. (currently amended) ~~An apparatus~~ A method for pulling a silicon single crystal using a silicon single crystal pulling apparatus comprising: a single crystal pulling chamber in which a carrier gas is supplied from above and exhausted from below; a crucible that is provided inside the single crystal pulling chamber, and into which a raw material is supplied and melted; and a heat shield that is disposed above the crucible, for guiding the carrier gas to a melt surface inside the crucible, in which the silicon single crystal is pulled from the melt inside the crucible, the heat shield being arranged to be raised and lowered,

~~Wherein the heat shield can be raised and lowered,~~ the method comprising:

positioning the heat shield ~~is positioned~~ where a carbon concentration inside the pulled silicon single crystal is 3×10^{15} atoms/cm^3 or less, and

pulling up the silicon single crystal ~~is pulled~~ while a growth condition V/G (V: growth rate, G: axial temperature gradient of the crystal) is adjusted such that void defects, OSFs (oxidation induced stacking faults), and dislocation clusters (interstitial silicon dislocation defects) are eliminated from the pulled silicon single crystal.

22. (new) In a method for manufacturing a silicon wafer to lessen the size of void defects, in which a silicon crystal is pulled from a silicon melt, a silicon wafer is acquired from the pulled silicon crystal, and in which the silicon crystal is pulled in a state in which the axial temperature gradient G_1 near the melting point of the silicon crystal is increased and a solid-liquid interface, comprising a boundary between the silicon crystal and the melt during the pulling of the silicon crystal, is convex with respect to the melt surface, the improvement comprising:

pulling the silicon crystal while maintaining the growth condition V/G_1 (where V is a growth rate of the pulled silicon crystal) in a range of values in a region of the pulled silicon crystal in which a size of a void defect becomes smaller, and is a range of values larger than a value of V/G_2 of a void defect region (where G_2 is an axial temperature gradient in a void defect region of the pulled silicon crystal and an OSF (Oxidation Induced Stacking Faults region).

23. (new) In a method for manufacturing a silicon wafer to lessen the size of void defects,

in which a silicon crystal is pulled from a silicon melt, a silicon wafer is acquired from the pulled silicon crystal, and in which the silicon crystal is pulled in a state in which the axial temperature gradient G_1 near the melting point of the silicon crystal is increased and a solid-liquid interface, comprising a boundary between the silicon crystal and the melt during the pulling of the silicon crystal, is convex with respect to the melt surface, the improvement comprising:

pulling the silicon crystal while maintaining the growth condition V/ G_1 (wherein V is a growth rate of the pulled silicon crystal) in a range of values in a region of the pulled silicon crystal in which a size of a void defect becomes smaller, and is a range of values smaller than a value of $V.G_2$ of a void defect region (where G_2 is an axial temperature gradient in a void defect region of the pulled silicon crystal).